

The Commissioner for PatentsREMARKS

The Examiner has rejected claims 1-30 under 35 U.S.C. 102(e) as being anticipated by US patent 6,515,678 to Boger. The Examiner is asked to reconsider the rejection for the following reasons.

At page 5, item (7) of the office action dated 09/08/2003, the Examiner has incorrectly labeled the "display controller system" with reference numeral "900". The Applicant would like to point out that the reference teaches reference number "900" to be the "digital information appliance" (column 7, line 10 and figure 9), which refers to the entire architecture of the system, including the main memory 904, the message bus 910, the network interface 906, and the display 914. The "processing system" (including the CPU and also identified as "a controller") is identified as "902", and the "display system" is identified as "912". As a result, there are several misrepresentations in the office action of 09/08/2003 which render the Examiner's rejection unclear and ambiguous. However, the Applicant has argued the rejection by making certain assumptions about what was intended by the Examiner. The Applicant requests the Examiner to respond in a non-final action if these assumptions do not correspond to what was intended by the Examiner.

On page 7 of the same office action, and with reference to claim 1, the Examiner has stated that the step of "in said display controller system, scaling said portion of said main surface in the frame buffer memory" can be found in the teachings of Boger by saying that "the display controller 900 performs the scaling process rather than the host system, column 6 line 66 to column 7 line 10 and column 8 lines 59-63". While it is incorrect to say that it is "the display controller 900" that performs the scaling, the Applicant fully agrees with the Examiner if the statement is meant to be that "the controller 902 performs the scaling process". The Applicant understands the scaling to be done by the controller 902 at the application level, as is commonly done in conventional systems. In contrast, as is clearly indicated by the claim language of claim 1 of the present invention, the step of scaling the portion of the main surface in the frame buffer memory is done in the display controller system. If the system of the

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present invention were to be compared with the architecture of figure 9 of Boger, the display controller system, as recited in the claims, is analogous to the display system 912. According to the description, the scaling of the system described by Boger is not done in the display system 912, but rather in the processing system 902. Therefore, this step of claim 1 is not found in Boger and the reference does not anticipate claim 1.

Additionally, the Examiner has also stated that the step of "in said display controller system, converting said scaled portion of said main surface in the frame buffer memory into a display signal", recited in claim 1 of the present application, is taught by Boger because "a display signal is formed by controller 900 and sent to display 914". Again, the Applicant points out that it is incorrect to identify the controller as 900. However, the Applicant believes the display signal is formed by processing system 902 to be sent to display 914. This again contrasts with the language of claim 1 of the present application, where it clearly recites that the conversion of the scaled portion be done in the display controller system. As evidenced by the above, claim 1 is not anticipated by Boger.

With respect to claim 21 of the present application, the Examiner has rejected the claim on the basis that the limitation of "receiving user input defining coordinates of a fractional portion of said main surface in the frame buffer memory to be scaled and displayed, said fractional portion being a non-integer fraction of said main surface of the frame buffer memory" is met by the user-defined area 622, column 6, lines 26-29, thus the user defines the area to be any size. The Applicant respectfully disagrees with this statement. The cited portion of the reference is reproduced as follows: "As shown in FIG. 6B, the selected portion may then be displayed in a user-defined area 622. In this way, the user may view details in the user-defined area 622 that were viewable in the high resolution". It is incorrect to assume that the user-defined area 622 could be a non-integer fractional portion of the main surface.

Boger does not explicitly state that the user-defined area 622 is an integer fraction of the total area because it is implicit that this be the case. No prior art has been cited by the Examiner to indicate that it was known, at the time Boger was filed, to be capable of selecting non-integer fractional portions of a main surface in a frame buffer

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memory. In addition, the background of the invention of the present application explicitly states the following:

"It is also known in the art to provide a single display controller hardware zoom in which the zoom operates to scale a fixed portion of a main surface memory, such as, for example, an area which is one quarter the size of the main surface memory, in which each pixel of the main surface memory is displayed as four pixels in the zoom display. The portion of the main surface memory can be displaced or dragged using the mouse. The known hardware zoom does not provide for a user defined magnification ratio to be used, and is limited to a fixed or a set of pre-defined magnification ratios." (page 2, lines 15-22).

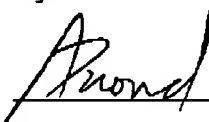
Even though the user uses a mouse to select a portion of the main surface and it appears that this portion is "user-defined", it is actually limited to fractional portions which are integer fractions of the main surface. Therefore, unless evidence to the contrary is provided, it should be rightfully assumed that the user-defined area respects integer fractional portions of the main surface.

In view of the foregoing, a Notice of Allowance for claims 1-30 is respectfully requested.

Respectfully submitted,

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